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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/802,203	03/17/2004	Roy J. Blazek	34282	3763

7590 07/05/2007

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EXAMINER	
GREEN, PHILLIP	

ART UNIT	PAPER NUMBER
2823	

MAIL DATE	DELIVERY MODE
07/05/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/802,203	BLAZEK ET AL.	
	Examiner	Art Unit	
	Phillip S. Green	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Fukuta et al. (US 2004/0144476 A1).

Re claim 1, Fukuta discloses a method of creating a monolithic circuit structure, the method comprising the steps of:

printing a circuit component onto an individual layer of substrate; (Note: Paragraph 0040)

firing the individual layer of substrate and the circuit component placed thereon; (Note: Paragraph 0041)

adjusting the circuit component as necessary to achieve a desired degree of precison; (Note: Paragraph 0043)

applying a bonding agent to the individual layer of substrate and assembling the individual layer of substrate with one or more other layers of substrate; and (Note: Paragraph 0045)

firing the assembled individual layer of substrate and one or more other layers of substrate together to activate the bonding agent, thereby bonding the individual layer of

substrate to the one or more other layers of substrate and creating the monolithic circuit structure. (Note: Paragraph 0048).

Re claim 2, Fukuta discloses all the claimed limitation according to Claim 1 in the paragraph above, including, wherein the circuit component is selected from the group consisting of: resistors, capacitors, and inductors. (Note: Paragraph 0040).

Re claim 3, Fukuta discloses all the claimed limitation according to Claim 1 in the paragraph above, including, wherein the circuit component is placed onto the individual layer of substrate by screen-printing. (Note: Paragraph 0036).

Re claim 4, Fukuta discloses all the claimed limitation according to Claim 1 in the paragraph above, including, wherein the individual layer of substrate and the one or more other layers of substrate are pre-fired thick film ceramic substrate. (Note: Paragraph 0041).

Re claim 5, Fukuta discloses all the claimed limitation according to Claim 1 in the paragraph above, including, wherein the individual layer of substrate and the one or more other layers of substrate are standard alumina thick film ceramic substrates. (Note: Paragraph 0028).

Re claim 6, Fukuta discloses all the claimed limitation according to Claim 1 in the paragraph above, including, wherein the bonding agent is a thick film glass. (Note: Paragraph 0028).

Re claim 7, Fukuta discloses a method of creating a monolithic circuit structure, the method comprising the steps of:

printing a circuit component onto an individual layer of substrate; (Note: Paragraph 0040)

firing the individual layer of thick film ceramic substrate and the circuit component printed thereon; (Note: Paragraph 0041)

trimming the circuit component as necessary to achieve a desired degree of precison; (Note: Paragraph 0043)

applying a bonding agent to the individual layer of thick film ceramic substrate and assembling the individual layer of thick film ceramic substrate with one or more other layers of thick film ceramic substrate; and (Note: Paragraph 0028-0045)

firing the assembled individual layer of thick film ceramic substrate and one or more other layers of thick film ceramic substrate together to activate the bonding agent, thereby bonding the individual layer of thick film ceramic substrate to the one or more other layers of thick film ceramic substrate and creating the multi- layered monolithic circuit structure. (Note: Paragraph 0028- 0048)

Re claim 8, Fukuta discloses all the claimed limitation according to Claim 7 in the paragraph above, wherein the plurality of circuit components are selected from the group consisting of: resistors, capacitors, and inductors. (Note: Paragraph 0040).

Re claim 9, Fukuta discloses all the claimed limitation according to Claim 7 in the paragraph above, wherein the individual layers of thick film ceramic substrate are standard alumina thick film ceramic substrate. (Note: Paragraph 0028).

Re claim 10, Fukuta discloses all the claimed limitation according to Claim 7 in the paragraph above, wherein the bonding agent is a thick film glass. (Note: Paragraph 0028).

Re claim 11, Fukuta discloses a method of creating a multi-layered monolithic circuit structure, the method comprising the steps of:

screen-printing a plurality of circuit components onto a plurality of individual layers of thick film ceramic substrate;

firing the individual layers of thick film ceramic substrate and the circuit components screen-printed thereon;

applying a thick film glass bonding agent to the individual layers of thick film ceramic substrate and assembling the individual layers of thick film ceramic substrate; and

firing the assembled individual layers of thick film ceramic substrate to sinter the thick film glass bonding agent, thereby bonding the individual layers of thick film ceramic substrate together and creating the multi-layered monolithic circuit structure. (Note: Paragraph 0028-0045)

Re claim 12, Fukuta discloses all the claimed limitation according to Claim 11 in the paragraph above, wherein the plurality of circuit components are selected from the group consisting of: resistors, capacitors, and inductors. (Note: Paragraph 0040).

Re claim 13, Fukuta discloses all the claimed limitation according to Claim 11 in the paragraph above, wherein the individual layers of thick film ceramic substrate are standard alumina thick film ceramic substrate. (Note: Paragraph 0028).

Re claim 14, Fukuta discloses a method of creating a multi-layered monolithic circuit structure, the method comprising the steps of:

screen-printing a plurality of circuit components onto a plurality of individual layers of substrate, wherein the circuit components are selected from the group consisting of: resistors, capacitors, and inductors, and wherein the individual layers of substrate are standard alumina thick film ceramic substrate;

firing the individual layers of substrate and the circuit components screen-printed thereon;

laser-trimming the circuit component as necessary to achieve a desired degree of precison;

applying a thick film glass bonding agent to the individual layers of substrate and assembling the individual layers of substrate; and

firing the assembled individual layers of substrate to sinter the thick film glass bonding agent, thereby bonding the individual layers of substrate together and creating the multi-layered monolithic circuit structure. (Note: Paragraph 0028- 0048).

Response to Arguments

3. Applicant's arguments with respect to claims 1-14 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

4. This action is made NON-FINAL.

Correspondence

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phillip S. Green whose telephone number is 571-272-7024. The examiner can normally be reached on Monday thru Thursday 9:30 am to 7:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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06/23/2005

Brook Kebede
BROOK KEBEDE
PRIMARY EXAMINER